	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030188286 A1	20031002	47	Method and Apparatus for Using a Diagona Line to Measure Congestion in a Region of an Integrated-Circuit Layout	716/13
2	US 20030088841 A1	20030508	50	Partitioning placement method and apparatus	716/8
3	US 20020170027 A1	20021114	56	Method and apparatus for pre-computing placement costs	716/10
4	US 20020157075 A1	20021024	56	Method and apparatus for computing placement costs	716/10
5	US 20020133798 A1	20020919	44	Method and apparatus for considering diagonal wiring in placement	716/10
6	US 20020073390 A1	20020613	44	Method and apparatus for using a diagonal line to measure an attribute of a bounding box of a net	716/8
7	US 20020069397 A1	20020606	56	Method and apparatus for placing circuit modules	716/12
8	US 20010038612 A1	20011108	53	Automatic routing system for circuit layout	370/256
9	US 6678872 B2	20040113	44	Method and apparatus for using a diagonal line to measure congestion in a region of an integrated-circuit layout	716/7
10	US 6671864 B2	20031230	45	Method and apparatus for using a diagonal line to measure an attribute of a bounding box of a net	716/8
11	US 6516455 B1	20030204	48	Partitioning placement method using diagonal cutlines	716/7

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12	US 6407434 B1	20020618	136	Hexagonal architecture	257/401
13	US 6312980 B1	20011106	134	Programmable triangular shaped device having variable gain	438/197
14	US 6097073 A	20000801	138	Triangular semiconductor or gate	257/401
15	US 5973376 A	19991026	136	Architecture having diamond shaped or parallelogram shaped cells	257/401

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16	US 5889329 A	19990330	139	Tri-directional interconnect architecture for SRAM	257/758
17	US 5872380 A	19990216	136	Hexagonal sense cell architecture	257/369
18	US 5864165 A	19990126	141	Triangular semiconductor NAND gate	257/401
19	US 5834821 A	19981110	140	Triangular semiconductor "AND" gate device	257/401

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20	US 5822214 A	19981013	135	CAD for hexagonal architecture	716/10
21	US 5811863 A	19980922	136	Transistors having dynamically adjustable characteristics	257/401
22	US 5808330 A	19980915	136	Polydirectional non-orthoginal three layer interconnect architecture	257/208
23	US 5801422 A	19980901	139	Hexagonal SRAM architecture	257/369

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24	US 5789770 A	19980804	136	Hexagonal architecture with triangular shaped cells	257/206
25	US 5777360 A	19980707	137	Hexagonal field programmable gate array architecture	257/315
26	US 5742086 A	19980421	136	Hexagonal DRAM array	257/300